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**IN THE CLAIMS:**

**Kindly amend claims 27, 28, 29, 31, 32, 33, cancel claims 34-35, and add new claims 36-48, all without prejudice, as follows:**

- note*
27. (Amended) An integrated circuit semiconductor device including  
a substrate having a substrate surface,  
a flowable oxide insulator (FOX) layer upon said substrate surface,  
a trough in said flowable oxide insulator layer,  
sidewalls of said flowable oxide insulator layer,  
a primary protective layer on said sidewalls of said flowable oxide insulator layer, said  
primary protective layer being a thin oxidized surface of said FOX, said thin surface layer  
preventing the exposure of said flowable oxide insulator layer to moisture and lithographic  
resist developers, said primary protective layer being substantially impervious to copper  
extrusion, and  
a secondary protective layer on said primary protective layer and on said substrate  
surface, said secondary protective layer being electrically conductive.
- Q1*
- SUB  
D1*
28. (Amended) The integrated circuit semiconductor device as claimed in claim 27,  
further comprising,  
an oxide layer upon said oxidized FOX layer,  
a conductor in said trough, said conductor and said oxide layer forming a planar  
surface, said conductor being in electrical communication with said secondary protective  
layer, and

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C1

~~a nitride layer upon said planar surface.~~

29. (Amended) The integrated circuit semiconductor device as claimed in claim 28, further comprising a damascene layer, said damascene layer comprising,
- another flowable oxide insulator (FOX) layer upon said nitride layer,
  - another thin oxidized surface layer of said another FOX layer,
  - another trough in said another FOX layer,
  - another sidewalls of said another flowable oxide insulator layer in said another trough,
  - another primary protective layer upon said another sidewalls, said another primary protective layer being said another thick oxidized surface layer preventing the exposure of said another flowable oxide insulator layer to moisture and lithographic resist developers, said another primary protective layer being impervious to copper extrusion,
  - another secondary protective layer upon said another primary protective layer and upon said even planar surface, said another secondary protective layer being in electrical communication with said conductor, and
  - another conductor in said another trough, said another conductor being in electrical communication with said another secondary protective layer.
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31. (Amended) The integrated circuit semiconductor device as claimed in claim 27, further comprising a nitride supplemental protective layer on said primary protective layer for improving adhesion with a metallic conductor.
32. (Amended) The integrated circuit semiconductor device as claimed in claim 27, wherein said primary layer is a barrier layer.

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33. (Amended) The integrated circuit semiconductor device as claimed in claim 27, wherein said primary protective layer on said sidewalls of said flowable oxide insulator layer has a thickness equal to or less than 20% of a thickness of said flowable oxide insulator layer

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34. (Canceled) ✓

35. (Canceled) ✓

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36. (New) The integrated circuit device of claim 31, wherein said supplemental protective layer is a nitride layer.

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37. (New) The integrated layer of claim 27, wherein said thin layer of plasma-formed oxide has a thickness not exceeding about 500 Å.

38. (New) An integrated circuit including  
a layer of flowable oxide insulator, and  
a thin protective layer thereon, said thin protective layer being an oxidized surface layer of said flowable oxide insulator that is resistant to moisture and lithographic resist developers.

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39. (New) The integrated circuit of claim 38, wherein said thin oxidized layer has a thickness less than about 500 Å.

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40. (New) The integrated circuit of claim 38, wherein said thin oxidized layer is a plasma-formed layer.

41. (New) The integrated circuit of claim 38, further including a nitride or oxynitride layer on said thin oxidized surface layer.

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42. (New) The integrated circuit of claim 38, further including a deposited oxide layer deposited on said thin oxidized surface layer.

43. (New) The integrated circuit of claim 38, further including a conductive layer on said thin oxidized surface layer.

44. (New) The integrated circuit of claim 43, further including a metal conductor in contact with said conductive barrier layer.

45. (New) The integrated circuit of claim 44, wherein said metal conductor contains copper.

46. (New) The integrated circuit of claim 45, wherein said conductive barrier layer includes a refractory metal or alloy.

47. (New) The integrated circuit of claim 46, wherein said layer of flowable oxide insulator is located between two non coplanar metal layers used for interconnections in said